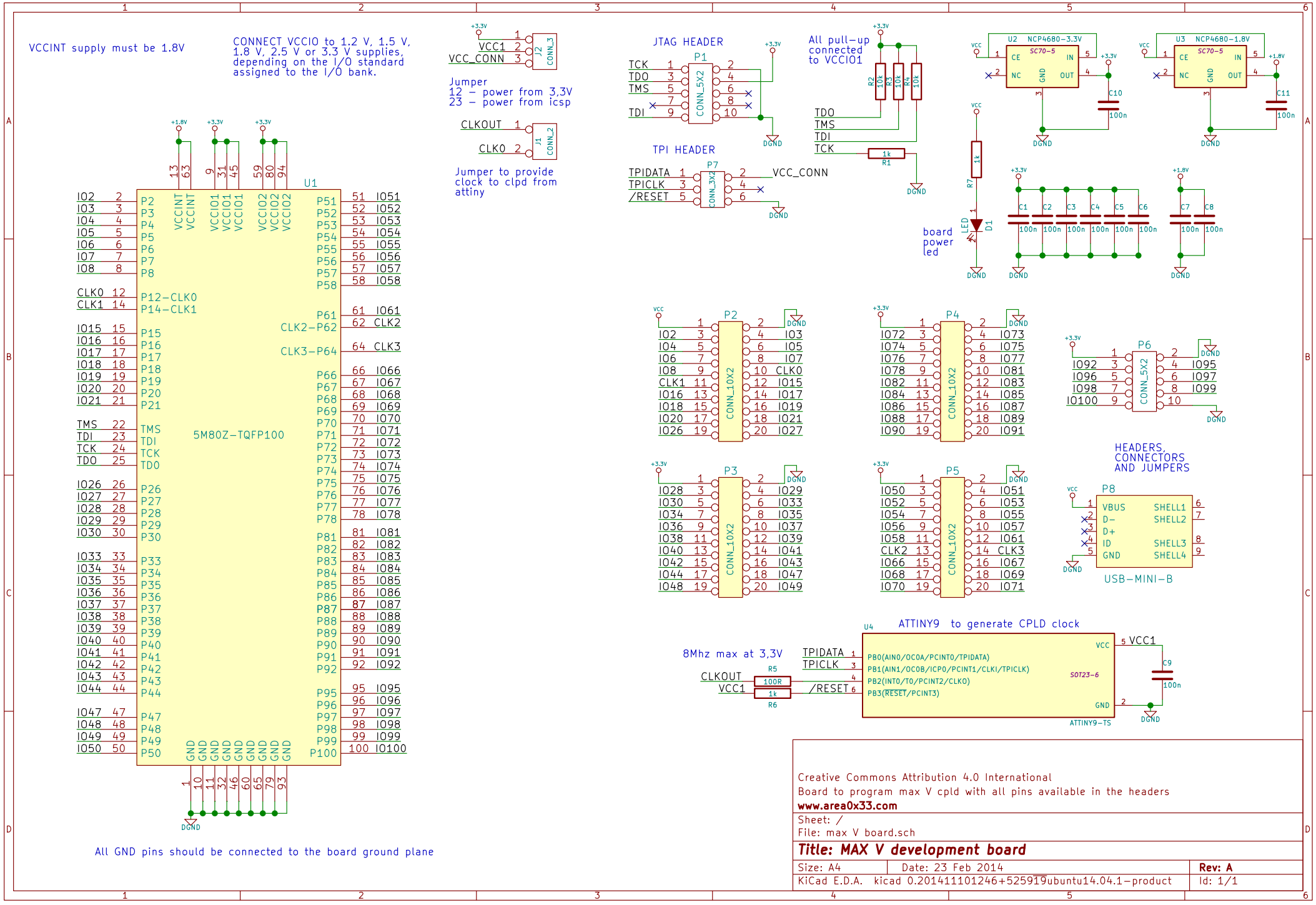
VCCINT supply must be 1.8V
CONNECT VCCIO to 1.2 V, 1.5 V, 1.8 V, 2.5 V or 3.3 V supplies, depending on the I/O standard assigned to the I/O bank.
U1
5M80Z-TQFP100
All GND pins should be connected to the board ground plane
J2 CONN_3
VCC1
VCC_CONN
Jumper
12 - power from 3,3V
23 - power from icsp
J1 CONN_2
CLKOUT
CLK0
Jumper to provide clock to clpd from attiny
JTAG HEADER
P1 CONN_5X2
TCK
TDO
TMS
TDI
TPI HEADER
P7 CONN_3X2
TPIDATA
TPICLK
/RESET
All pull-up connected to VCCIO1
R2 10k
R3 10k
R4 10k
R1 1k
U2 NCP4680-3.3V
U3 NCP4680-1.8V
SC70-5
CE
NC
GND
IN
OUT
C10 100n
C11 100n
R7 1k
D1 LED
board power led
C1 C2 C3 C4 C5 C6 100n
C7 C8 100n
P2 CONN_10X2
P3 CONN_10X2
P4 CONN_10X2
P5 CONN_10X2
P6 CONN_5X2
HEADERS, CONNECTORS AND JUMPERS
P8
VBUS
D-
D+
ID
GND
SHELL1
SHELL2
SHELL3
SHELL4
USB-MINI-B
U4
ATTINY9 to generate CPLD clock
8Mhz max at 3,3V
R5 100R
R6 1k
PB0(AIN0/OC0A/PCINT0/TPIDATA)
PB1(AIN1/OC0B/ICP0/PCINT1/CLKI/TPICLK)
PB2(INT0/T0/PCINT2/CLKO)
PB3(RESET/PCINT3)
SOT23-6
ATTINY9-TS
C9 100n
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Board to program max V cpld with all pins available in the headers
www.area0x33.com
Sheet: /
File: max V board.sch
Title: MAX V development board
Size: A4
Date: 23 Feb 2014
Rev: A
KiCad E.D.A. kicad 0.201411101246+525919ubuntu14.04.1-product
Id: 1/1